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EXAMINER	
RASHID, DAVID	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,193	JEONG ET AL.	
	Examiner	Art Unit	
	David P. Rashid	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,14 and 15* is/are rejected.

7)☒ Claim(s) *10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

All of the examiner's suggestions presented herein below have been assumed for examination purposes, unless otherwise noted.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) (Application # 10-2003-0006102, filed 1/22/2004), which papers have been placed of record in the file.

2. MPEP §201.13 II G states "An applicant may incorporate by reference the foreign priority application by including, in the U.S. application-as-filed, an explicit statement that such specifically enumerated foreign priority application or applications are "hereby incorporated by reference." The statement must appear in the specification. See 37 CFR 1.57(b) and MPEP §608.01(p)." – it is suggested to incorporate by reference the foreign priority application by including an explicit statement in the specification.

Claim Rejections - 35 USC § 112

3. **Claim 1** defines applicant's invention in a "means plus function" format, reciting a "mean for" followed by functional language, and not limited by structure. Thus, "means plus function" is automatically invoked (*In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994); Refer to MPEP 2181*). However, in order to invoke mean plus function, the 35 U.S.C. 112, second paragraph requirements must be met (MPEP 2181, IDENTIFYING A 35 U.S.C. 112, SIXTH PARAGRAPH LIMITATION). The MPEP 2163 and 2181 state, and supports with the applicable law, the following:

> If a claim limitation invokes 35 U.S.C. 112, para. 6, it must be interpreted to cover the corresponding structure, materials, or acts in the specification and "equivalents thereof." See 35 U.S.C. 112, para. 6. See also *B. Braun Medical, Inc. v. Abbott Lab.*, 124 F.3d 1419, 1424, 43 USPQ2d 1896, 1899 (Fed. Cir. 1997). In considering whether there is 35 U.S.C. 112, para. 1 support for a means- (or step) plus-function claim limitation, the examiner must consider not only the original disclosure contained in the summary and detailed description of the invention portions of the specification, but also the original claims, abstract, and drawings.

> 35 U.S.C. 112, sixth paragraph states that a claim limitation expressed in means-plus-function language "shall be construed to cover the corresponding structure... described in the specification and equivalents thereof." "If one employs means plus function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112." *In re Donaldson Co.*, 16 F.3d 1189, 1195, 29 USPQ2d 1845, 1850 (Fed. Cir. 1994) (in banc).

and

> A means- (or step-) plus-function claim limitation is adequately described under 35 U.S.C. 112, para. 1, if: (1) The written description adequately links or associates adequately described particular structure, material, or acts to the function recited in a means- (or step-) plus-function claim limitation; or (2) it is clear based on the facts of the application that one skilled in the art would have known what structure, material, or acts perform the function recited in a means- (or step-) plus-function limitation. Note also: A rejection under 35 U.S.C. 112, para. 2, "cannot stand where there is adequate description in the specification to satisfy 35 U.S.C. 112, first paragraph, regarding means-plus-function recitations that are not, per se, challenged for being unclear." *In re Noll*, 545 F.2d 141, 149, 191 USPQ 721, 727 (CCPA 1976).

Upon reviewing applicant's original disclosure (i.e., specification, claims and drawings), it is the examiner's conclusion that the written description does not link or associate particular structure to the function recited in the means-plus-function claim limitations, and it is not clear based on the facts of the application that one skilled in the art would have known what structure or materials perform the function recited in a means-plus-function limitation.

Claim 1 recites the phrases "image processing means for converting the left and right image to a left and a right digital image". The specification only refers to a generalized system for performing this function and cites an "image processing unit", as depicted in FIG.1. The specification fails to provide any specifics regarding the structure of these generalized functional blocks. The specification does not describe the specific structure of the apparatus. However,

since no function is specified by the word(s) preceding "means," it is impossible to determine the equivalents of the element, as required by 35 U.S.C. 112, sixth paragraph. See *Ex parte Klumb*, 159 USPQ 694 (Bd. App. 1967). It is suggested to replacing "image processing means" to "image processing unit" in claim 1, line 6, and all other occurrences in the dependent claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1 – 5, 7 – 9,** and **14 - 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Onda (US 5,867,591 A) in view of Jeong et al. (US 2002/0025075 A1).

Regarding **claim 1**, while Onda discloses a multi-layered real-time stereo matching system (FIG. 22) comprising:

a left and a right image acquisition means ("right and left cameras" in Col. 10, lines 41 – 54) for obtaining a left (FIG. 22, element S1601) and a right (FIG. 22, element S1602) image on a spatial area from different position (distance between elements 23L and 23R in FIG. 1); and

a multi-layered image matching means (FIG. 22, element S1605) for comparing one scan line ("left window TLk(x,y)" in FIG. 17; left window in FIG. 16, element TL1) in one of the left and the right digital image with multiple scan lines ("right window TLk(x,y)" in FIG. 17; right window in FIG. 16, element TR1; Col. 6, lines 29 – 40) in the other of the left and the right digital image in real-time so that each pixel ("similarity evaluation result" in FIG. 17; Col. 6,

lines 41 - 60) in the one scan line matches another pixel in the multiple scan lines in the other digital image, Onda does not disclose an image processing means for converting the left and the right image to a left and a right digital image (though the images of Ondo are digital as disclosed).

Jeong discloses a system for matching stereo image in real time (FIG. 1) that includes an image processing means (FIG. 1, element 12) for converting the left and the right image to a left ("left image" in FIG. 1) and a right ("right image" in FIG. 1) digital image.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the multi-layered real-time stereo matching system on Ondo to include an image processing means for converting the left and the right image to a left and a right digital image as taught by Jeong "to provide a real-time stereo image matching system which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", Jeong, paragraph [0008].

Regarding **claim 2**, while Ondo in view of Jeong discloses the system of claim 1, Ondo includes wherein the multi-layered image matching means (FIG. 22, element S1605) receives pixels of the one scan line (pixels in "left window TLk(x,y)" in FIG. 17; left window in FIG. 16, element TL1) in the one digital image (FIG. 22, element S1601) sequentially and receives pixels (pixels in "right window TRk(x,y)" in FIG. 17; window in FIG. 16, element TR1) of the multiple scan lines (right window in FIG. 16, element TR1 with right and left arrows attached; Col. 6, lines 29 – 40) in the other digital image (FIG. 22, element S1602) at a time (left window in FIG. 16, element TR1 does not depict right and left arrows attached), and calculates a disparity between one pixel in the one scan line ("similarity evaluation result" in FIG. 17;"disp1" and

"disp2" in FIG. 18; Col. 14, lines 23 – 31) and said another pixel in the multiple scan lines (FIG. 20).

Regarding **claim 3**, while Ondo in view of Jeong discloses the system of claim 2, Ondo discloses wherein the multi-layered image matching means includes:

a plurality of layers ("u=1", "u=2", ... "u=8", as well as "BL(X – 1, Y)"... "BL(X+1,Y)" in FIG. 18 with respect to storing "disp1" and "disp2" from each comparison between the left and right windows) for receiving the one scan line ("left window TLk(x,y)" in FIG. 17; left window in FIG. 16, element TL1) in the one digital image (FIG. 22, element S1601) and receiving the multiple scan lines ("right window TLk(x,y)" in FIG. 17; right window in FIG. 16, element TR1; Col. 6, lines 29 – 40) in the other digital image (FIG. 22, element S1602) one by one, wherein two adjacent layers exchange costs and active signals with each other (Col. 15, lines 35 – 48 with respect to "disp1" and "disp2" stored in the layers that are "exchanging costs and active signals" by adding in a histogram to determine a peak value; FIG. 20); and

an accumulator (Col. 15, lines 35 – 48; FIG. 20) for accumulating data fed from the layers to generate the disparity ("disparity of block..." in Col. 15, lines 49 – 51).

Regarding **claim 4**, while Ondo in view of Jeong discloses the system of claim 3, and while Ondo discloses wherein each of the layers has: a first storing means (pixels in "left window TLk(x,y)" in FIG. 17 must have memory) for storing pixels of the left digital image (FIG. 22, element S1601); and a second storing means (pixels in "right window TRk(x,y)" in FIG. 17 must have memory) for storing pixels of the right digital image (FIG. 22, element S1602), Ondo does not disclose having a plurality of forward processors, stacks and backward

processors for generating decision values and the disparity obtained from the left and the right digital image based on a clock signal.

Jeong discloses a system for matching stereo image in real time (FIG. 1) that includes wherein each scan line has:

a first storing means (FIG. 1, element 12) for storing pixels of the left digital image ("Lin" in FIG. 3);

a second storing means (FIG. 1, element 12) for storing pixels of the right digital image ("Rin" in FIG. 3); and

a forward processor (FIG. 3, element 30), stack (FIG. 3, element 31) and backward processor (FIG. 3, element 32) for generating decision values ("decision value" in paragraph [0023]) and the disparity ("disparity" in paragraph [0023]) obtained from the left and the right digital image based on a clock signal ("Clock" in FIG. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for each layer of Ondo in view of Jeong to include having a forward processor, stack and backward processor for generating decision values and the disparity obtained from the left and the right digital image based on a clock signal (thus a plurality of forward processors, stacks and backward processors for all layers) as taught by Jeong "to provide a real-time stereo image matching system which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", Jeong, paragraph [0008].

Regarding **claim 5**, while Ondo in view of Jeong disclose the system of claim 4, Ondo does not teach wherein each of the forward processors of said each of the layers contains: a first

multiplexor for determining a minimum cost among a recursive cost within said each of the forward processors and two costs fed from an upper and a lower layer of said each of the layers; a first cost register for storing the minimum cost; an absolute value calculator for calculating as a matching cost a difference between one of the pixels of the first image storing means and another pixel of the pixels of the second image storing means; a first adder for adding the matching cost to the minimum cost to generate a first added cost, a second multiplexor for deciding a minimum cost among the first added cost and two costs fed from an upper and a lower forward processor in said each of the layers; a second cost register for storing the minimum cost fed from the second multiplexor, wherein the minimum cost is fed back to the first cost multiplexor as the recursive cost and also provided to the upper and the lower layer; and a second adder for adding the minimum cost stored in the second cost register to an occlusion cost to provide a second added cost to the upper and the lower forward processor.

Jeong discloses a system for matching stereo image in real time (FIG. 1) that includes wherein each of the forward processors (FIG. 3, element 30; FIG. 2, element 22) of each scan line contains:

a first multiplexor (FIG.5, element 43) for determining a minimum cost among a recursive cost within said each of the forward processors and two costs fed from an upper and a lower layer of said each scan line (paragraphs [0025], [0027]);

a first cost register (FIG. 4, element 44) for storing the minimum cost (paragraph [0025]);

an absolute value calculator (FIG. 4, element 41) for calculating as a matching cost a difference between one of the pixels of the first image storing means and another pixel of the pixels of the second image storing means (paragraph [0025]);

a first adder (FIG. 4, element 42) for adding the matching cost to the minimum cost to generate a first added cost (paragraph [0025]),

a second multiplexor (FIG. 4, element 43) for deciding a minimum cost among the first added cost and two costs ("Uin2" and "Uin1" in FIG. 4) fed from an upper and a lower forward processor in said each of the layers (paragraphs [0045], [0046]);

a second cost register (FIG. 4, element 44) for storing the minimum cost fed from the second multiplexor, wherein the minimum cost is fed back to the first cost multiplexor as the recursive cost and also provided to the upper and the lower layer (paragraph [0047]); and

a second adder (FIG. 4, element 42) for adding the minimum cost stored in the second cost register to an occlusion cost to provide a second added cost to the upper and the lower forward processor (paragraph [0045]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for each layer of Ondo in view of Jeong to include wherein each of the forward processors of said each of the layers contains: a first multiplexor for determining a minimum cost among a recursive cost within said each of the forward processors and two costs fed from an upper and a lower layer of said each of the layers; a first cost register for storing the minimum cost; an absolute value calculator for calculating as a matching cost a difference between one of the pixels of the first image storing means and another pixel of the pixels of the second image storing means; a first adder for adding the matching cost to the minimum cost to generate a first added cost, a second multiplexor for deciding a minimum cost among the first added cost and two costs fed from an upper and a lower forward processor in said each of the layers; a second cost register for storing the minimum cost fed from the second multiplexor, wherein the

minimum cost is fed back to the first cost multiplexor as the recursive cost and also provided to the upper and the lower layer; and a second adder for adding the minimum cost stored in the second cost register to an occlusion cost to provide a second added cost to the upper and the lower forward processor as taught by Jeong "to provide a real-time stereo image matching system which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", Jeong, paragraph [0008].

Regarding **claim 7**, while Ondo in view of Jeong discose the system of claim 3, Ondo discloses wherein each of the layers ("u=1", "u=2", ... "u=8", as well as "BL(X – 1, Y)"... "BL(X+1,Y)" in FIG. 18 with respect to storing "disp1" and "disp2" from each comparison between the left and right windows) is inputted with pixels (storing values "disp1" and "disp2" come from pixels of one scan line as shown in FIG. 17) of one scan line ("left window TLk(x,y)" in FIG. 17; left window in FIG. 16, element TL1) of the one digital image (FIG. 22, element S1601) and pixels (storing values "disp1" and "disp2" come from pixels from the other multiple scan lines as shown in FIG. 17) of multiple scan lines ("right window TLk(x,y)" in FIG. 17; right window in FIG. 16, element TR1; Col. 6, lines 29 – 40) of the other digital image (FIG. 22, element S1602).

Regarding **claim 8**, while Ondo in view of Jeong disclose the system of claim 5, Ondo does not disclose wherein all the cost registers except a 0-th cost register in the forward processors in said each of the layers is initialized with maximum cost, respectively, and the second storing means is initialized based on the right digital image.

Jeong discloses a system for matching stereo image in real time (FIG. 1) that includes wherein all the cost registers except a 0-th cost register in the forward processors in said each of the layers is initialized with maximum cost, respectively, and the second storing means is initialized based on the right digital image (paragraph [0039]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for each layer of Ondo in view of Jeong to include wherein all the cost registers except a 0-th cost register in the forward processors in said each of the layers is initialized with maximum cost, respectively, and the second storing means is initialized based on the right digital image as taught by Jeong "to provide a real-time stereo image matching system which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", Jeong, paragraph [0008].

Regarding **claim 9**, while Ondo in view of Jeong disclose the system of claim 5, Ondo does not teach wherein,

if a sum of a processing element number and a forward processing step number is an even number, said each of the forward processors decides a minimum cost among the recursive cost and two added costs obtained by adding the occlusion cost to said two costs fed from the upper and the lower forward processor in said each of the layers, respectively, to provide the minimum cost as a first decision value to a stack,

and, if otherwise, said each of the forward processors determines another minimum cost among a cost obtained by adding an absolute pixel difference of the left and the right digital

image to the first decision value and two costs of two forward processors of the upper and the lower layer to provide the minimum cost as a second decision value to the stack.

Jeong discloses a system for matching stereo image in real time (FIG. 1) that includes wherein

if a sum of a processing element number and a forward processing step number is an even number, said each of the forward processors decides a minimum cost among the recursive cost and two added costs obtained by adding the occlusion cost to said two costs fed from the upper and the lower forward processor in said each of the layers, respectively, to provide the minimum cost as a first decision value to a stack (paragraphs [0036], [0037]; "If i + j is even" and its full condition in paragraph [0063]),

and, if otherwise, said each of the forward processors determines another minimum cost among a cost obtained by adding an absolute pixel difference of the left and the right digital image to the first decision value and two costs of two forward processors of the upper and the lower layer to provide the minimum cost as a second decision value to the stack (paragraphs [0036], [0037]; "If i + j is odd" and its full condition in paragraph [0063]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for each layer of Ondo in view of Jeong to include wherein, if a sum of a processing element number and a forward processing step number is an even number, said each of the forward processors decides a minimum cost among the recursive cost and two added costs obtained by adding the occlusion cost to said two costs fed from the upper and the lower forward processor in said each of the layers, respectively, to provide the minimum cost as a first decision value to a stack, and, if otherwise, said each of the forward processors determines another

minimum cost among a cost obtained by adding an absolute pixel difference of the left and the right digital image to the first decision value and two costs of two forward processors of the upper and the lower layer to provide the minimum cost as a second decision value to the stack as taught by Jeong "to provide a real-time stereo image matching system which enables real-time stereo matching, by parallel processing video image sequences using an algorithm which is based on a new trellis based method and is optimal in the Bayesian sense.", Jeong, paragraph [0008].

Regarding **claim 14**, claim 1 recites identical features as in claim 14. Thus, references/arguments equivalent to those presented above for claim 1 are equally applicable to claim 14.

Regarding **claim 15**, while Ondo in view of Jeong disclose the system of claim 14, Ondo discloses wherein the step (b) includes the steps of:

(b1) determining a path of a minimum cost as a decision value ("disp1" and "disp2" in FIG. 18; Col. 14, lines 23 – 31) based on pixel data of the one scan line (pixels in "left window TLk(x,y)" in FIG. 17) and pixel data of the multiple scan lines (pixels in "right window TRk(x,y)" in FIG. 17; right window in FIG. 16, element TR1; Col. 6, lines 29 – 40);

(b2) calculating a disparity ("identify most-frequent-valued block as true disparity" in FIG. 19; Col. 15, lines 35 – 51) from the decision value; and

(b3) using the disparity to find a pair of pixels from the left and the right digital image and calculating a distance from the disparity (once the block disparity is found, the distance between the right and left windows is itself "disp" as shown in FIG. 16).

Allowable Subject Matter

6. **Claims 6 – 13** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding **claims 6 – 13**, while the prior art teaches backward processors as those disclosed by Ondo in view of Jeong in claim 4, the prior art does not teach wherein each of the backward processors of said each of the layers includes: an OR gate for logically summing two active bit paths inputted from an upper and a lower backward processor in said each of the layers, two active bit paths inputted from an upper and a lower layer of said each of the layers and a recursive active bit path within said each of the backward processors to generate a logical sum of five active bit paths; an activation register for storing the logical sum of five active bit paths; a demultiplexor for demultiplexing the logical sum of five active bit paths based on a decision value fed from the stack; and a tri-state buffer for outputting the decision value in case the logical sum of five active bit paths in the activation register is high.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David P. Rashid whose telephone number is (571) 270-1578. The examiner can normally be reached Monday - Friday 8:30 - 17:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David P. Rashid/
Examiner, Art Unit 2624

David P Rashid
Examiner
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/Brian P. Werner/
Supervisory Patent Examiner (SPE), Art Unit 2624